The TCD2964BFG is a high sensitive and low dark current 21360 elements × 6 line CCD color image sensor. The sensor is designed for scanner.

The device contains a row of 21360 elements × 6 line staggered photodiodes which provide a 192 lines/mm (4800 DPI) across a A4 size paper. The device is operated by 5 V pulse and 12 V power supply.

Features

- Number of Image Sensing Elements: 21360 elements × 6 line
- Image Sensing Element Size: 2 μm by 4 μm on 2 μm centers
- Photo Sensing Region: High sensitive and low dark current PN photodiode
- Distance between Photodiode Array: 64 μm (32 lines), Red line-Green line, Green line-Blue line 6 μm (3 lines), Odd line-Even line
- Clock: 2 phase (5 V)
- Power Supply: 12 V Power Supply Voltage
- Package: 32pin CLCC package
- Color Filter: Red, Green, Blue
- Overflow drain for antiblooming

ABSOLUTE MAXIMUM RATINGS (Note 1)

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Symbol</th>
<th>Rating</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock pulse voltage</td>
<td>V₀</td>
<td>-0.3~8.0</td>
<td>V</td>
</tr>
<tr>
<td>Storage pulse voltage</td>
<td>VST</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Shift pulse voltage</td>
<td>VSH</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Reset pulse voltage</td>
<td>VRS</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Switch pulse voltage</td>
<td>VSW</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Storage pulse input voltage</td>
<td>VSTI</td>
<td>-3~15</td>
<td>V</td>
</tr>
<tr>
<td>Power supply voltage</td>
<td>VOD</td>
<td>-0.3~15</td>
<td>V</td>
</tr>
<tr>
<td>Operating temperature</td>
<td>Töpr</td>
<td>0~60</td>
<td>°C</td>
</tr>
<tr>
<td>Storage temperature</td>
<td>Tstg</td>
<td>-25~85</td>
<td>°C</td>
</tr>
</tbody>
</table>

Note 1: All voltage are with respect to SS terminals (ground).
None of the ABSOLUTE MAXIMUM RATINGS must be exceeded, even instantaneously.
If any one of the ABSOLUTE MAXIMUM RATINGS is exceeded, the electrical characteristics, reliability and life time of the device cannot be guaranteed.
If the ABSOLUTE MAXIMUM RATINGS are exceeded, the device can be permanently damaged or degraded.
Create a system design in such a manner that any of the ABSOLUTE MAXIMUM RATINGS will not be exceeded under any circumstances.
Pin Names

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Symbol</th>
<th>Name</th>
<th>Pin No.</th>
<th>Symbol</th>
<th>Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>OS3</td>
<td>Signal output 3 (red)</td>
<td>32</td>
<td>OS2</td>
<td>Signal output 2 (green)</td>
</tr>
<tr>
<td>2</td>
<td>SS</td>
<td>Ground</td>
<td>31</td>
<td>OS1</td>
<td>Signal output 1 (blue)</td>
</tr>
<tr>
<td>3</td>
<td>NC</td>
<td>Non connection</td>
<td>30</td>
<td>OD</td>
<td>Power</td>
</tr>
<tr>
<td>4</td>
<td>RS</td>
<td>Reset gate</td>
<td>29</td>
<td>SW</td>
<td>Switch gate</td>
</tr>
<tr>
<td>5</td>
<td>$\varphi_{1B}$</td>
<td>Final stage clock (phase 1)</td>
<td>28</td>
<td>$\varphi_{2B}$</td>
<td>Final stage clock (phase 2)</td>
</tr>
<tr>
<td>6</td>
<td>$\varphi_{1A2}$</td>
<td>Clock 2 (phase 1)</td>
<td>27</td>
<td>NC</td>
<td>Non connection</td>
</tr>
<tr>
<td>7</td>
<td>NC</td>
<td>Non connection</td>
<td>26</td>
<td>$\varphi_{2A2}$</td>
<td>Clock 2 (phase 2)</td>
</tr>
<tr>
<td>8</td>
<td>NC</td>
<td>Non connection</td>
<td>25</td>
<td>SS</td>
<td>Ground</td>
</tr>
<tr>
<td>9</td>
<td>STO</td>
<td>Storage pulse output</td>
<td>24</td>
<td>NC</td>
<td>Non connection</td>
</tr>
<tr>
<td>10</td>
<td>STI</td>
<td>Storage pulse input</td>
<td>23</td>
<td>NC</td>
<td>Non connection</td>
</tr>
<tr>
<td>11</td>
<td>SH3</td>
<td>Shift gate 3</td>
<td>22</td>
<td>SH4</td>
<td>Shift gate 4</td>
</tr>
<tr>
<td>12</td>
<td>SH2</td>
<td>Shift gate 2</td>
<td>21</td>
<td>SH1</td>
<td>Shift gate 1</td>
</tr>
<tr>
<td>13</td>
<td>$\varphi_{2A1}$</td>
<td>Clock 1 (phase 2)</td>
<td>20</td>
<td>NC</td>
<td>Non connection</td>
</tr>
<tr>
<td>14</td>
<td>NC</td>
<td>Non connection</td>
<td>19</td>
<td>$\varphi_{1A1}$</td>
<td>Clock 1 (phase 1)</td>
</tr>
<tr>
<td>15</td>
<td>NC</td>
<td>Non connection</td>
<td>18</td>
<td>NC</td>
<td>Non connection</td>
</tr>
<tr>
<td>16</td>
<td>SS</td>
<td>Ground</td>
<td>17</td>
<td>ST</td>
<td>Storage gate</td>
</tr>
</tbody>
</table>

Arrangement of the 1st Effective Pixel (S1)

Blue Photo Diode Arrays (21360 pixels x 2 line)

Green Photo Diode Arrays (21360 pixels x 2 line)

Red Photo Diode Arrays (21360 pixels x 2 line)
Optical/Electrical Characteristics

\( Ta = 25°C, V_{OD} = 12\, V, V_{\phi} = V_{RS} = 5\, V \) (pulse), \( V_{ST} = V_{SH} = 3.3\, V \) (pulse), \( f_{\phi} = 1\, MHz, f_{RS} = 2\, MHz, t_{INT} = 22\, ms, \) LIGHT SOURCE = A LIGHT SOURCE + CM500S FILTER \( t = 1\, mm, \) LOAD RESISTANCE = 100 kΩ

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ.</th>
<th>Max</th>
<th>Unit</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sensitivity</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Red</td>
<td>( R_{(R)} )</td>
<td>0.9</td>
<td>1.3</td>
<td>1.7</td>
<td>V/lx·s</td>
<td>(Note 2)</td>
</tr>
<tr>
<td>Green</td>
<td>( R_{(G)} )</td>
<td>1.0</td>
<td>1.5</td>
<td>2.0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Blue</td>
<td>( R_{(B)} )</td>
<td>0.4</td>
<td>0.7</td>
<td>1.0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Photometric Non-uniformity</td>
<td>PRNU (1)</td>
<td>—</td>
<td>10</td>
<td>20</td>
<td>%</td>
<td>(Note 3)</td>
</tr>
<tr>
<td></td>
<td>PRNU (3)</td>
<td>—</td>
<td>3</td>
<td>12</td>
<td>mV</td>
<td>(Note 4)</td>
</tr>
<tr>
<td>Register Imbalance</td>
<td>RI</td>
<td>—</td>
<td>1</td>
<td>3</td>
<td>%</td>
<td>(Note 5)</td>
</tr>
<tr>
<td>Saturation Output Voltage</td>
<td>( V_{SAT} )</td>
<td>2.4</td>
<td>2.8</td>
<td>—</td>
<td>V</td>
<td>(Note 6)</td>
</tr>
<tr>
<td>Saturation Exposure</td>
<td>SE</td>
<td>—</td>
<td>1.87</td>
<td>—</td>
<td>lx·s</td>
<td>(Note 7)</td>
</tr>
<tr>
<td>Dark Signal Voltage</td>
<td>( V_{DRK} )</td>
<td>—</td>
<td>0.6</td>
<td>2.7</td>
<td>mV</td>
<td>(Note 8)</td>
</tr>
<tr>
<td>Dark Signal Non-uniformity</td>
<td>DSNU</td>
<td>—</td>
<td>6.6</td>
<td>9.2</td>
<td>mV</td>
<td>(Note 8)</td>
</tr>
<tr>
<td>DC Power Dissipation</td>
<td>( P_D )</td>
<td>—</td>
<td>360</td>
<td>470</td>
<td>mW</td>
<td>—</td>
</tr>
<tr>
<td>Total Transfer Efficiency</td>
<td>TTE</td>
<td>92</td>
<td>98</td>
<td>—</td>
<td>%</td>
<td>—</td>
</tr>
<tr>
<td>Output Impedance</td>
<td>( Z_O )</td>
<td>—</td>
<td>0.2</td>
<td>0.5</td>
<td>kΩ</td>
<td>—</td>
</tr>
<tr>
<td>DC Output Voltage</td>
<td>( V_{OS} )</td>
<td>4.8</td>
<td>5.8</td>
<td>6.8</td>
<td>V</td>
<td>(Note 9)</td>
</tr>
<tr>
<td>Reset Noise</td>
<td>( V_{RSN} )</td>
<td>—</td>
<td>0.4</td>
<td>1.0</td>
<td>V</td>
<td>(Note 9)</td>
</tr>
<tr>
<td>Random Noise</td>
<td>( N_{D\sigma} )</td>
<td>—</td>
<td>0.7</td>
<td>—</td>
<td>mV</td>
<td>(Note 10)</td>
</tr>
</tbody>
</table>

Note 2: Sensitivity is defined for each color of signal outputs average when the photosensitive surface is applied with the light of uniform illumination and uniform color temperature.

Note 3: PRNU (1) is defined for each color on a single chip by the expressions below when the photosensitive surface is applied with the light of uniform illumination and uniform color temperature.

\[
PRNU (1) = \frac{\Delta x}{\bar{x}} \times 100\% 
\]

Where \( \bar{x} \) is average of total signal output and \( \Delta x \) is the maximum deviation from \( \bar{x} \). The amount of incident light is shown below.

Red = 1/2·SE
Green = 1/2·SE
Blue = 1/4·SE

Note 4: PRNU (3) is defined as maximum voltage with next pixels, where measured at 5% of SE (typ.).

Note 5: Register imbalance is defined as follows.

\[
RI = \frac{\sum_{n=1}^{42719} |x_{n} - x_{n+1}|}{42719 \times \bar{x}} \times 100\%
\]

Note 6: \( V_{SAT} \) is defined as minimum saturation output of all effective pixels.

Note 7: Definition of SE

\[
SE = \frac{V_{SAT}}{R_{G}} \quad (lx\cdot s)
\]
Note 8: $V_{DRK}$ and DSNU are defined at $t_{INT} = 14.55\text{ms}$.

$V_{DRK}$ is defined as average dark signal voltage of all effective pixels. DSNU is defined as different voltage between $V_{DRK}$ and $V_{MDK}$ when $V_{MDK}$ is maximum dark signal voltage.

Note 9: DC signal output voltage is defined as follows. Reset noise voltage is defined as follows.

Note 10: Random noise is defined as the standard deviation (sigma) of the output level difference between two adjacent effective pixels under no illumination (i.e. dark conditions) calculated by the following procedure.

1. Two adjacent pixels (pixel n and n + 1) after reference level clamp in one reading are fixed as measurement points.
2. Each of the output level at video output periods averaged over 200 ns period to get $V(n)$ and $V(n + 1)$.
3. $V(n + 1)$ is subtracted from $V(n)$ to get $\Delta V$.

$$\Delta V = V(n) - V(n + 1)$$

4. The standard deviation of $\Delta V$ is calculated after procedure (2) and (3) are repeated 30 times (30 readings).

$$\sigma = \sqrt{\frac{1}{30} \sum_{i=1}^{30} (\Delta V_i - \bar{\Delta V})^2}$$

5. Procedure (2), (3) and (4) are repeated 10 times to get sigma value.
6. 10 sigma values are averaged.

$$\bar{\sigma} = \frac{1}{10} \sum_{j=1}^{10} \sigma_j$$

7. $\bar{\sigma}$ value calculated using the above procedure is observed $\sqrt{2}$ times larger than that measured relative to the ground level. So we specify random noise as follows.

$$ND\sigma = \frac{1}{\sqrt{2}} \bar{\sigma}$$
Operating Condition

For best performance, the device should be used within the Recommended Operating Conditions.

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ.</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock pulse voltage</td>
<td>$V_{HA}$</td>
<td>4.5</td>
<td>5.0</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>$V_{LB}$</td>
<td>0</td>
<td>0</td>
<td>0.3</td>
<td>V</td>
</tr>
<tr>
<td>Final stage clock pulse</td>
<td>$V_{HB}$</td>
<td>4.5</td>
<td>5.0</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>voltage</td>
<td>$V_{LB}$</td>
<td>0</td>
<td>0</td>
<td>0.3</td>
<td>V</td>
</tr>
<tr>
<td>Storage pulse voltage</td>
<td>$V_{ST}$</td>
<td>2.7</td>
<td>3.3</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>$V_{ST}$</td>
<td>0</td>
<td>0</td>
<td>0.8</td>
<td>V</td>
</tr>
<tr>
<td>Shift pulse voltage</td>
<td>$V_{SH}$</td>
<td>2.7</td>
<td>3.3</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>$V_{SH}$</td>
<td>0</td>
<td>0</td>
<td>0.8</td>
<td>V</td>
</tr>
<tr>
<td>Reset pulse voltage</td>
<td>$V_{RS}$</td>
<td>4.5</td>
<td>5.0</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>$V_{RS}$</td>
<td>0</td>
<td>0</td>
<td>0.5</td>
<td>V</td>
</tr>
<tr>
<td>Switch pulse voltage</td>
<td>$V_{SW}$</td>
<td>2.7</td>
<td>3.3</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>$V_{SW}$</td>
<td>0</td>
<td>0</td>
<td>0.8</td>
<td>V</td>
</tr>
<tr>
<td>Power supply voltage</td>
<td>$V_{DD}$</td>
<td>11.4</td>
<td>12.0</td>
<td>12.6</td>
<td>V</td>
</tr>
</tbody>
</table>

Clock Characteristics ($Ta = 25^\circ C$)

For best performance, the device should be used within the Recommended Operating Conditions.

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ.</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock pulse frequency</td>
<td>$f_{p}$</td>
<td>0.15</td>
<td>1.0</td>
<td>11.0</td>
<td>MHz</td>
</tr>
<tr>
<td>Reset pulse frequency</td>
<td>$f_{RS}$</td>
<td>0.3</td>
<td>2.0</td>
<td>10.0</td>
<td>MHz</td>
</tr>
<tr>
<td>Clock capacitance</td>
<td>$C_{MA}$</td>
<td>—</td>
<td>225</td>
<td>—</td>
<td>pF</td>
</tr>
<tr>
<td>(Note 11)</td>
<td>$C_{MB}$</td>
<td>—</td>
<td>10</td>
<td>—</td>
<td>pF</td>
</tr>
<tr>
<td>Final Stage Clock capacitance</td>
<td>$C_{SB}$</td>
<td>—</td>
<td>30</td>
<td>—</td>
<td>pF</td>
</tr>
<tr>
<td>Storage gate capacitance</td>
<td>$C_{ST}$</td>
<td>—</td>
<td>20</td>
<td>—</td>
<td>pF</td>
</tr>
<tr>
<td>Shift gate capacitance</td>
<td>$C_{SH}$</td>
<td>—</td>
<td>10</td>
<td>—</td>
<td>pF</td>
</tr>
<tr>
<td>Reset gate capacitance</td>
<td>$C_{RS}$</td>
<td>—</td>
<td>20</td>
<td>—</td>
<td>pF</td>
</tr>
<tr>
<td>Switch gate capacitance</td>
<td>$C_{SW}$</td>
<td>—</td>
<td>10</td>
<td>—</td>
<td>pF</td>
</tr>
</tbody>
</table>

Note 11: $V_{OD} = 12$ V

Mode Select

<table>
<thead>
<tr>
<th>$SW$</th>
<th>Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>H</td>
<td>4800dpi mode</td>
</tr>
<tr>
<td>L</td>
<td>2400dpi mode 1200dpi mode 600dpi mode</td>
</tr>
</tbody>
</table>
Timing Chart 1 (4800DPI mode (1) )

ST

SH1

SH2

SH3 ("L")

SH4 ("L")

ϕ1A,B

ϕ2A,B

RS

SW ("H")

OS

DUMMY OUTPUTS (34 elements)

DUMMY OUTPUTS (12 elements)

DUMMY OUTPUTS (20 elements)

DUMMY OUTPUTS (34 elements)

DUMMY OUTPUTS (10727 elements)

DUMMY OUTPUTS (13 elements)

DUMMY OUTPUTS (8 elements)

DUMMY OUTPUTS (10680 elements)

DUMMY OUTPUTS (2 elements)

TEST OUTPUTS (2 elements)

DUMMY OUTPUTS (20 elements)

DUMMY OUTPUTS (8 elements)

DUMMY OUTPUTS (13 elements)

DUMMY OUTPUTS (1 element)
Timing Chart 2 (4800DPI mode (2))

- **ST** ("L")
- **SH1** ("L")
- **SH2**
- **SH3**
- **SH4** ("L")
- **Φ1A,B**
- **Φ2A,B**
- **RS**
- **SW** ("H")

**Signals:**
- **D1** to **D101**
- **S1** to **S32**
- **D19** to **D72**
- **S4** to **S12**
- **S11** to **S19**
- **S42707** to **S42716**

**Groups:**
- **DUMMY OUTPUTS** (34 elements)
- **DUMMY OUTPUTS (20 elements)
- **DUMMY OUTPUTS (12 elements)
- **DUMMY OUTPUTS (8 elements)
- **DUMMY OUTPUTS (13 elements)
- **LIGHT SHIELD OUTPUTS (10727 elements)
- **SIGNAL OUTPUTS (10680 elements)

**Notes:**
- **TEST OUTPUTS** (2 elements)
- **DUMMY OUTPUT** (1 element)
Timing Chart 3 (4800DPI mode (3) )

- **ST ("L")**
- **SH1 ("L")**
- **SH2 ("L")**
- **SH3**
- **SH4**
- **ϕ1A,B**
- **ϕ2A,B**
- **RS**
- **SW ("H")**

**Outputs:**
- **DUMMY OUTPUTS** (34 elements)
- **DUMMY OUTPUTS** (20 elements)
- **LIGHT SHIELD OUTPUTS** (12 elements)
- **SIGNAL OUTPUTS** (10680 elements)
- **TEST OUTPUTS** (2 elements)
- **DUMMY OUTPUTS** (8 elements)
- **DUMMY OUTPUTS** (13 elements)
- **DUMMY OUTPUT** (1 element)
Timing Chart 4 (4800DPI mode (4))

- **ST**
- **SH1**
- **SH2 ("L")**
- **SH3 ("L")**
- **SH4**
- **\(\Phi_{1A,B}\)**
- **\(\Phi_{2A,B}\)**
- **RS**
- **SW ("H")**

**Notes:**
- DUMMY OUTPUTS (34 elements)
- DUMMY OUTPUTS (20 elements)
- DUMMY OUTPUTS (12 elements)
- LIGHT SHIELD OUTPUTS (12 elements)
- SIGNAL OUTPUTS (10680 elements)
- DUMMY OUTPUTS (10727 elements)
- DUMMY OUTPUTS (8 elements)
- DUMMY OUTPUTS (13 elements)
- TEST OUTPUTS (2 elements)
- DUMMY OUTPUT (1 element)
Timing Chart 5 (2400DPI mode (1))

- ST
- SH1
- SH2
- SH3 ("L")
- SH4 ("L")
- φ₁A,B
- φ₂A,B
- RS
- SW ("L")

Diagram showing signal flow and timing with various labels and elements.
Timing Chart 6 (2400DPI mode (2))
Timing Chart 7 (2400DPI mode (3) )
Timing Chart 8 (2400DPI mode (4))
Timing Chart 9 (1200DPI mode (1))

- **ST**
- **SH1, SH2**
- **SH3, SH4**
- **ϕ1A, B**
- **ϕ2A, B**
- **RS**
- **SW (L)**

**OS**

- **DUMMY OUTPUTS (10 elements)**
- **LIGHT SHIELD OUTPUTS (6 elements)**
- **DUMMY OUTPUTS (17 elements)**
- **SIGNAL OUTPUTS (5340 elements)**
- **DUMMY OUTPUTS (4 elements)**
- **DUMMY OUTPUTS (7 elements)**
- **TEST OUTPUT (1 element)**
- **DUMMY OUTPUT (1 element)**

(5364 elements)
Timing Chart 10 (1200DPI mode (2) )

ST

SH1, SH2

SH3, SH4

ϕ1A, B

ϕ2A, B

RS

SW ("L")

OS

DUMMY OUTPUTS (10 elements)
LIGHT SHIELD OUTPUTS (6 elements)
SIGNAL OUTPUTS (5340 elements)
DUMMY OUTPUTS (17 elements)
DUMMY OUTPUTS (5364 elements)
DUMMY OUTPUTS (4 elements)
DUMMY OUTPUTS (7 elements)

TEST OUTPUT (1 element)
DUMMY OUTPUT (1 element)
Timing Chart 11 (600DPI mode)

ST

SH1, SH2

SH3, SH4

$\phi_{1A,B}$

$\phi_{2A,B}$

RS

SW ("L")
Timing Requirements

**ST, \( \overline{SW} \) Timing**

![Timing diagram for ST, \( \overline{SW} \) Timing]

**\( \phi_1, \phi_2 \) Cross point**

![Timing diagram for \( \phi_1, \phi_2 \) Cross point]

**ST, SH, \( \phi_1A \), RS Timing (4800DPI / 2400DPI Mode)**

![Timing diagram for ST, SH, \( \phi_1A \), RS Timing]

Note 12: Set the voltage level of RS to “L” level.

**SH, \( \phi_1A \), \( \phi_2A \) Timing (4800DPI / 2400DPI Mode)**

![Timing diagram for SH, \( \phi_1A \), \( \phi_2A \) Timing]

3.5 V (max) 1.5 V (min)
ST, SH, ϕ1A, RS Timing (1200DPI Mode)

ST, SH, ϕ1A, RS Timing (600DPI Mode)

Note 12: Set the voltage level of RS to “L” level.

SH, ϕ2A Timing (1200DPI Mode)

Note 12: Set the voltage level of RS to “L” level.

ST, SH, ϕ1A, ϕ2A Timing (600DPI Mode)

Note 12: Set the voltage level of RS to “L” level.
$\phi_1, \phi_2, \text{RS, OS Timing (4800DPI Mode)}$

$\phi_1, \phi_2, \text{RS, OS Timing (2400DPI / 1200DPI / 600DPI Mode)}$
Timing Requirements

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ. (Note 13)</th>
<th>Max</th>
<th>Unit</th>
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<tbody>
<tr>
<td>ST pulse rise time, fall time</td>
<td>t1, t3</td>
<td>0</td>
<td>50</td>
<td>—</td>
<td>ns</td>
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<tr>
<td>ST pulse width</td>
<td>t2</td>
<td>3000</td>
<td>5000</td>
<td>—</td>
<td>ns</td>
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<tr>
<td>SW pulse rise time, fall time</td>
<td>t4</td>
<td>0</td>
<td>50</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>Pulse timing of ST and SW</td>
<td>t5</td>
<td>0</td>
<td>0</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>SH pulse rise time, fall time</td>
<td>t6, t8</td>
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<td>50</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>SH pulse width</td>
<td>t7</td>
<td>3000</td>
<td>5000</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>Pulse timing of ST and SH</td>
<td>t9</td>
<td>3000</td>
<td>5000</td>
<td>—</td>
<td>ns</td>
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<tr>
<td>Pulse timing of ST and $\phi_{1A}$</td>
<td>t10</td>
<td>110</td>
<td>1000</td>
<td>—</td>
<td>ns</td>
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<tr>
<td>Pulse timing of ST and $\phi_{2A}$</td>
<td>t11</td>
<td>110</td>
<td>1000</td>
<td>—</td>
<td>ns</td>
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<tr>
<td>Pulse timing of SH and $\phi_{1A}$</td>
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<td>1000</td>
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<td>ns</td>
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<tr>
<td>Pulse timing of SH and $\phi_{2A}$</td>
<td>t13</td>
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<td>5000</td>
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<td>ns</td>
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<tr>
<td>Pulse timing of SH and RS</td>
<td>t14</td>
<td>110</td>
<td>1000</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>Pulse timing of SH and $\phi_{1B}$</td>
<td>t15</td>
<td>3000</td>
<td>5000</td>
<td>—</td>
<td>ns</td>
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<tr>
<td>RS pulse rise time, fall time</td>
<td>t16</td>
<td>0</td>
<td>500</td>
<td>—</td>
<td>ns</td>
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<tr>
<td>$\phi_{1}, \phi_{2}$ pulse rise time, fall time</td>
<td>t17, t18</td>
<td>0</td>
<td>50</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>RS pulse width</td>
<td>t19, t21</td>
<td>0</td>
<td>20</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>Pulse timing of $\phi_{1B}, \phi_{2B}$ and RS</td>
<td>t22</td>
<td>15</td>
<td>100</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>Video data delay time</td>
<td>t23, t24</td>
<td>—</td>
<td>25</td>
<td>—</td>
<td>ns</td>
</tr>
</tbody>
</table>

Note 13: Typ. is the case of $f_{\phi} = 1.0$ MHz.

Note 14: Load resistance is 100 $k\Omega$.

Typical Spectral Response

![Spectral response graph](image_url)
Typical Drive Circuit

IC1, 2: TC74AC04P
TR1, 2, 3: 2SC1815-Y
R1: 150 Ω
R2: 1500 Ω
Caution

1. Electrostatic Breakdown

   Store in shorting clip or in conductive foam to avoid electrostatic breakdown.

   CCD Image Sensor is protected against static electricity, but inferior puncture mode device due to static electricity is sometimes detected. In handling the device, it is necessary to execute the following static electricity preventive measures, in order to prevent the trouble rate increase of the manufacturing system due to static electricity.

   a. Prevent the generation of static electricity due to friction by making the work with bare hands or by putting on cotton gloves and non-charging working clothes.

   b. Discharge the static electricity by providing earth plate or earth wire on the floor, door or stand of the work room.

   c. Ground the tools such as soldering iron, radio cutting pliers of or pincer.

      It is not necessarily required to execute all precaution items for static electricity.
      It is all right to mitigate the precautions by confirming that the trouble rate within the prescribed range.

   d. Ionized air is recommended for discharge when handling CCD image sensors.

2. Incident Light

   CCD sensor is sensitive to infrared light. Note that infrared light component degrades resolution and PRNU of CCD sensor.

3. Cloudiness of Glass Inside

   CCD surface mount products may have a haze on the inside of glass, so be careful about following.
   Even if the haze arises inside of glass, when it is not on the pixel area, there is no problem in quality.

   a. Before the aluminum bag is opened, please keep the products in the environment below 30°C90%RH.
      And after the aluminum bag is opened, please keep the products in the environment below 30°C60%RH.

   b. Please mount the products within 12month from sealed date and within 6 month from opening the aluminum bag. (Sealed date is printed on aluminum bag.)

4. Ultrasonic Cleaning

   Ultrasonic cleaning should not be used with such hermetically-sealed ceramic package as CCD because the bonding wires can become disconnected due to resonance during the cleaning process.

5. Mounting

   In the case of solder mounting, the devices should be mounted with the window glass protective tape in order to avoid dust or dirt included in reflow machine.

6. Window Glass Protective Tape

   The window glass protective tape is manufactured from materials in which static charges tend to build up. When removing the tape from CCD sensor after solder mounting, install an ionizer to prevent the tape from being charged with static electricity.

   When the tape is removed, adhesives will remain in the glass surface. Since these adhesives appear as black or white flaws on the image, please wipe the window glass surface with the cloth into which the organic solvent was infiltrated. Then please attach CCD to a product.

   Do not reuse the tape.
7. **Soldering Temperature Profile for Pb free**

Good temperature profile for each soldering method is as follows. In addition, in case of the repair work accompanied by IC removal, since the degree of parallel may be spoiled with the left solder, please do not carry out and in case of the repair work not accompanied by IC removal, carry out with a soldering iron or, in reflow, only one time.

a. **Using a soldering iron**
   Complete soldering within ten seconds for lead temperatures of up to 260°C, or within three seconds for lead temperatures of up to 350°C.

b. **Using long infrared rays reflow / hot air reflow**
   Please do reflow at the condition that the package surface (electrode) temperature is on the solder maker's recommendation profile. And that reflow profile is within below condition 1 to 3.

1. Peak temperature: 250°C or less.
2. Time to keep high temperature: 220~250°C, 30~40sec.
3. Pre. heat: 150~190°C, 60~120sec

8. **Window Glass**

   The dust and stain on the glass window of the package degrade optical performance of CCD sensor.

   Keep the glass window clean by saturating a cotton swab in alcohol and lightly wiping the surface, and allow the glass to dry, by blowing with filtered dry N2. Care should be taken to avoid mechanical or thermal shock because the glass window is easily to damage.

9. **Cleaning Method of the Window Glass Surface**

   **Wiping Cloth**
   a. Use soft cloth with a fine mesh.
   b. The wiping cloth must not cause dust from itself.
   c. Use a clean wiping cloth necessarily.

   Recommended wiping cloth is as follow:
   · MK cloth (Toray Industries)

   **Cleaner**
   Recommended cleaning liquid of window glass are as follow:
   · EE-3310 (Olympus)

   When using solvents, such as alcohol, unavoidably, it is cautious of the next.
   a. A clean thing with quick-drying.
   b. After liquid dries, there needs to be no residual substance.
   c. A thing safe for a human body.

   And, please observe the use term of a solvent and use the storage container of a solvent to be clean.
   Be cautious of fire enough.

   **Way of Cleaning**
   First, the surface of window glass is wiped with the wiping cloth into which the cleaner was infiltrated. Please wipe down the surface of window glass at least 2 times or more.
   Next, the surface of window glass wipes with the dry wiping cloth. Please wipe down the surface of window glass at least 3 times or more.

   Finally, blow cleaning is performed by dry N2 filtered.
   If operator wipes the surface of the window glass with the above-mentioned process and dirt still remains, Toshiba recommends repeating the clean operation from the beginning.
   Be cautious of the next thing.
   a. Don't infiltrate the cleaner too much.
   b. A wiping portion is performed into the optical range and don't touch the edge of window glass.
   c. Be sure to wipe in a long direction and the same direction.
   d. A wiping cloth always uses an unused portion.
10. Foot Pattern on the PCB

We recommend fig1’s foot pattern for your PCB (Printed circuit Board).

11. Mask for Solder Paste Application

We recommend metal mask that have the following thickness.

- TCD****BFG (Pad material: Au): a thickness of 0.2mm.

And we recommend that the size of the pattern of the metal mask is 95% to 100% of recommended foot pattern at fig1.

12. Temperature cycle

After mounting, if temperature cycle stress is too much, CCD surface mount products have a possibility that a crack may arise in solder. As a method of preventing a solder crack, underfil is effective.

13. Reuse of a Tray

We reuse tray in order to reduce plastic waste as we can. Please cooperate with us in reusing for ecology.
14. Caution for Package Handling

Over force on CCD products may cause crack and chip removing on the product. The three point bending strength of this product is the following. (Reference data)

If the stress is loaded far from a fulcrum, the stress on the package will be increase.

When you will treat CCD on every process, please be careful particularly. For example, soldering on PCB, cutting PCB, wiping on the glass surface, optical assemble and so on.

![bending test](image)

- 32CLCC
  - Bearing length 19mm: The force from upside: 250[N]
  - Bearing length 50mm: The force from upside: 120[N]

15. Dummy Scan

The device cannot output normal signal immediately after power-on. Execute 20lines of dummy scan to obtain normal signal output.
Weight: 3.2 g (typ.)
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Overflow Drain Performance

Specified as below.
No blooming when exposed 4.45 times the exposure that gives 2.4V of output voltage at t\text{INT}=22ms and exposed area on CCD=9.6mm.

Chip Warpage

Specified as 0 +/- 20 [um] by the definition below. This specification is based on the actual distribution. No inspection is performed for the products.

(Definition)
In the figure below, chip warpage is defined as the vertical distance of Z3 from the line connecting Z1 and Z2 (datum).
When Z3 is at cover glass side from the datum, the sign is defined as "+".
When Z3 is at package side from the datum, the sign is defined as "-".
Chip warpage is defined by the product before solder mounting on PCB.

Chip Slope

Specified as follows by the definition below.
0 +/- 0.25 [degree] for longer direction
0 +/- 2 [degree] for shorter direction
This specification is based on the actual distribution. No inspection is performed for the products.

(Definition)
In the figure below, chip slope is calculated by Z1, Z2, \cdots, Z6 value from bottom of package.
for longer direction: Chip slope is defined by Z1 and Z5 and by Z2 and Z6.
When Z5>Z1 or Z6>Z2, the sign is defined as "+".
When Z5<Z1 or Z6<Z2, the sign is defined as "-".
for shorter direction: Chip slope is defined by Z1 and Z2, by Z3 and Z4 and by Z5 and Z6.
When Z1>Z2 or Z3>Z4 or Z5>Z6, the sign is defined as "+".
When Z1<Z2 or Z3<Z4 or Z5<Z6, the sign is defined as "-".
Chip slope is defined by the product before solder mounting on PCB.
## Change history

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<tr>
<th>Rev.</th>
<th>Date</th>
<th>Description</th>
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<td>1</td>
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<td>changed warning ABSOLUTE MAXIMUM RATINGS, Operating Condition, Clock Characteristics</td>
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